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2. [Phase Locked Loops \[31K\]](#)

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3. [POWER ADAPTIVE FREQUENCY DIVIDER](#)

VAUCHER, Cicero S. / VEREJKEN, Hubertus, H., M., PATENT COOPERATION TREATY APPLICATION, Nov 2001

...divider cell. Such a frequency divider is known from Application Note 4 Using the
PE3291/92 in CDMA Applications'from Peregrine Semiconductor Corporation. The
PE3291 is a fractional-N PLL integrated frequency synthesizer and contains two
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4. [Power adaptive frequency divider](#)

Vaucher, Cicero Silveira / Vereijken, Hubertus Hendrikus Martinus, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Dec 2002

...divider cell. Such a frequency divider is known from Application Note 4 'Using the
PE3291/92 in CDMA Applications' from Peregrine Semiconductor Corporation. The
PE3291 is a fractional-N PLL integrated frequency synthesizer and contains two
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Inventor Information for 10/664850

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
10664850	Not Issued	30	09/22/2003	Method and apparatus to generate signals using two or more phase locked loops	REUVEN, YOSSI
60641398	Not Issued	159	01/04/2005	Wired networking	REUVEN, YOSSI
60659913	Not Issued	159	03/10/2005	Access network	REUVEN, YOSSI
60682820	Not Issued	159	05/20/2005	Multi drop DSL	REUVEN, YOSSI
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